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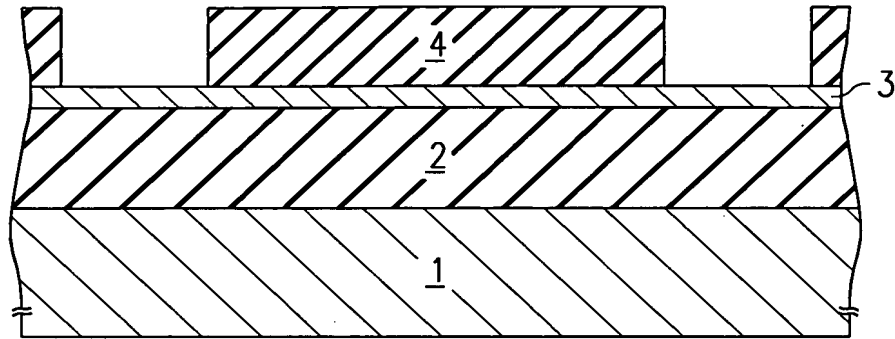


FIG. 1

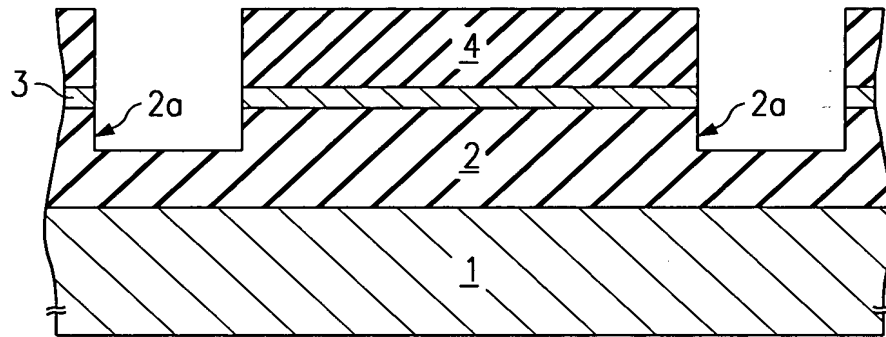


FIG. 2

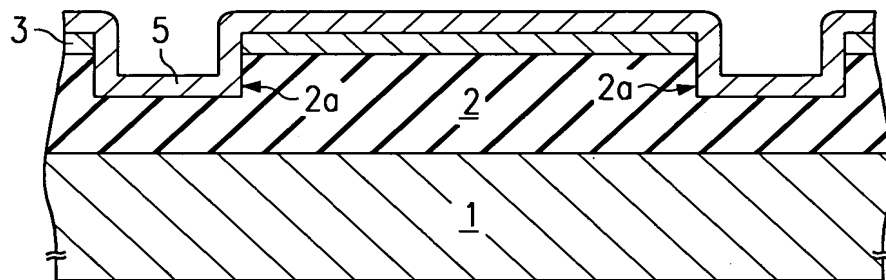


FIG. 3

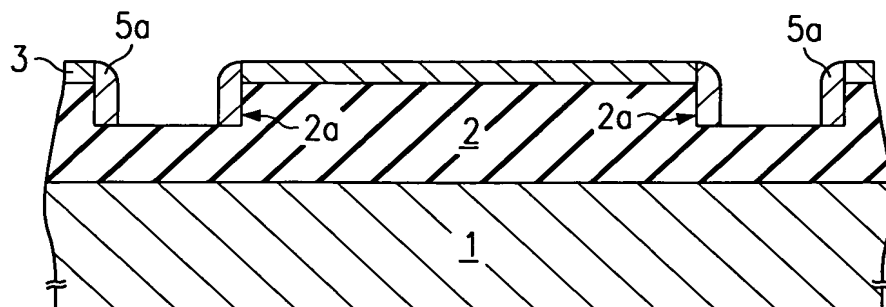


FIG. 4

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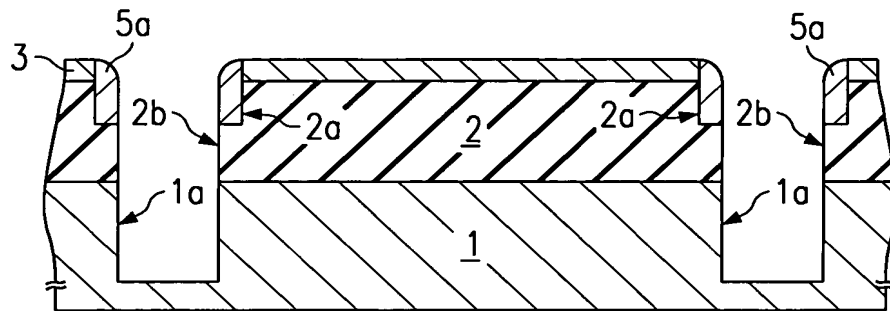


FIG. 5

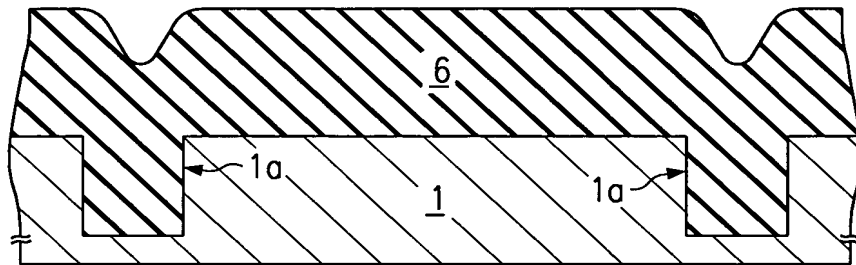


FIG. 6

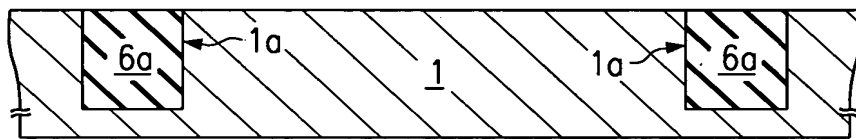


FIG. 7

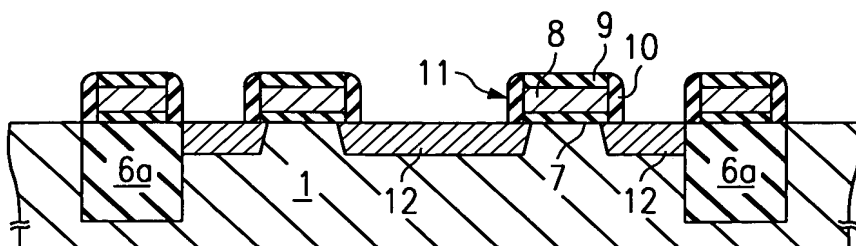
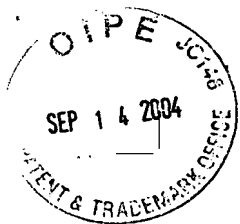


FIG. 8



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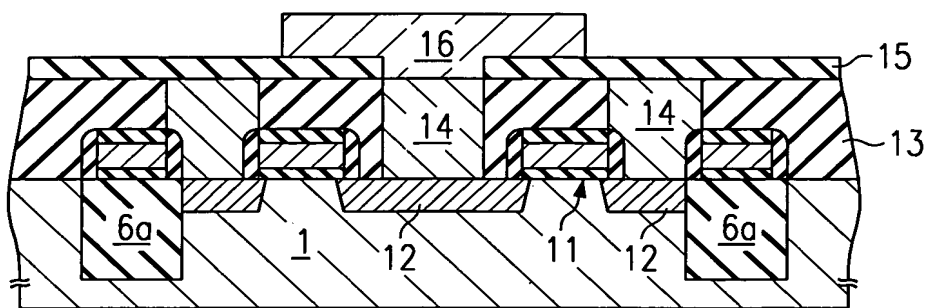


FIG. 9

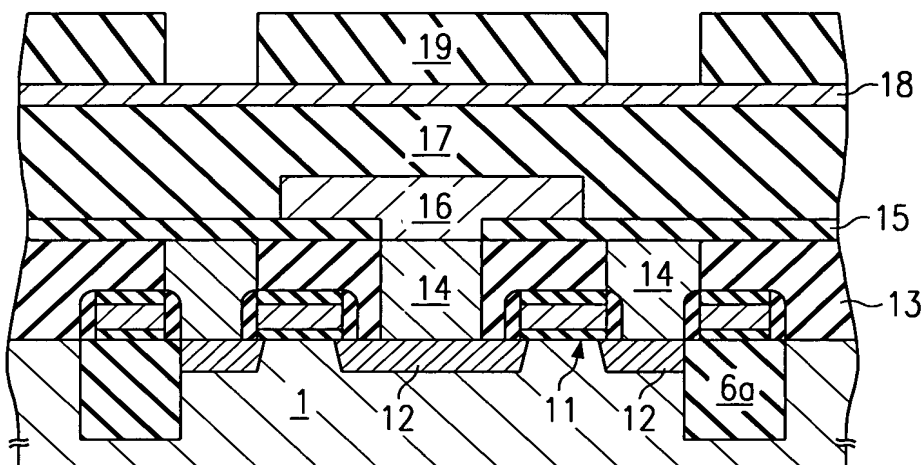


FIG. 10

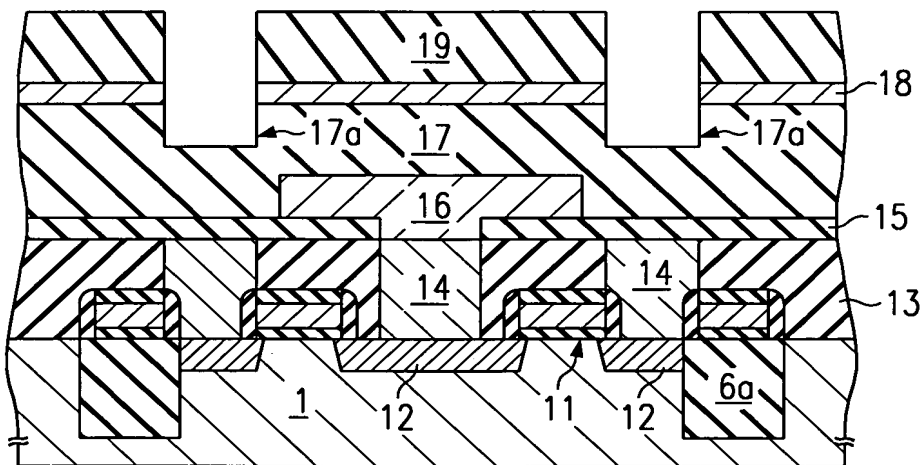


FIG. 11

This cross-sectional view illustrates a semiconductor device with a complex multi-layered architecture. The structure is built upon a substrate (1) and includes several key layers and components:

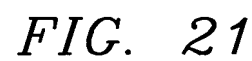
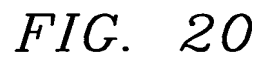
- Substrate (1):** The base layer of the device.
- Gate Stack (11, 12):** Located at the bottom, consisting of a gate dielectric (11) and a gate electrode (12).
- Source/Drain Regions (14):** Doped regions on either side of the gate stack.
- Channel Region (16):** The central region of the device where carrier transport occurs.
- Interlayer Dielectric (15):** A dielectric layer covering the source/drain and channel regions.
- Conductive Layers (17, 17a):** Multiple layers of conductive material, with 17a indicating a specific sub-layer or pattern.
- Passivation Layer (21):** A protective layer on top of the conductive layers.
- Interconnects (22):** Conductive lines used for electrical connections between different parts of the device.
- Dielectric Layers (23, 24):** Additional dielectric layers used for insulation and protection.
- Top Layers (25, 26, 26a):** The uppermost layers of the device, including a top dielectric (25) and a top conductive layer (26).
- Contacts (27, 28):** Pads or openings at the top surface for external electrical connections.

FIG. 17



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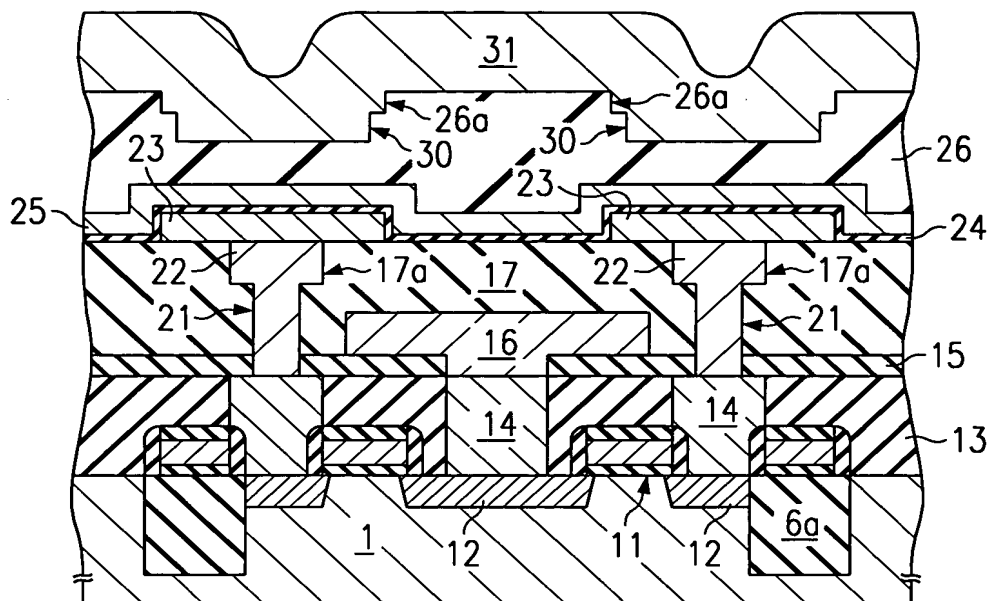


FIG. 22

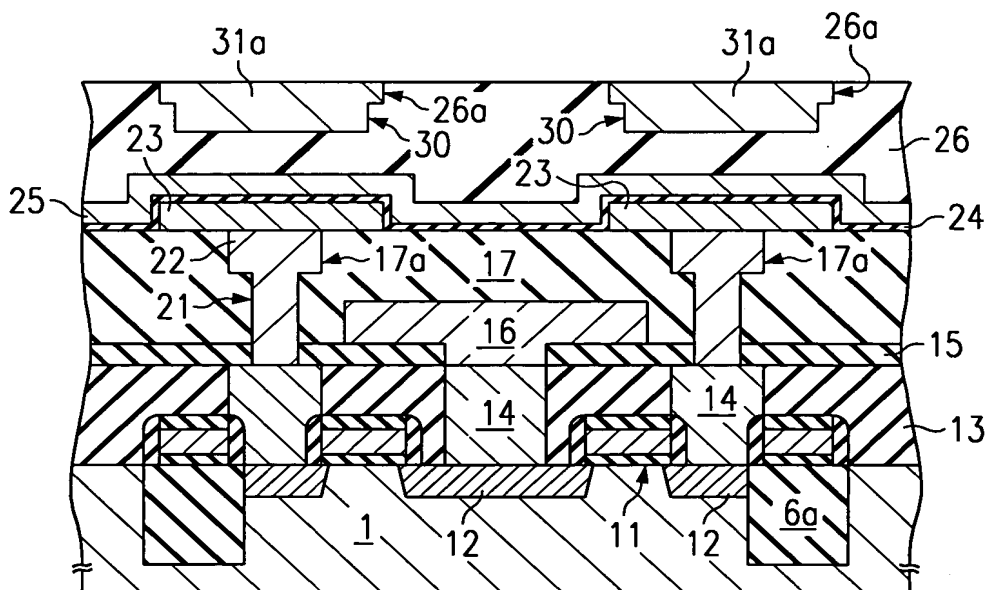


FIG. 23